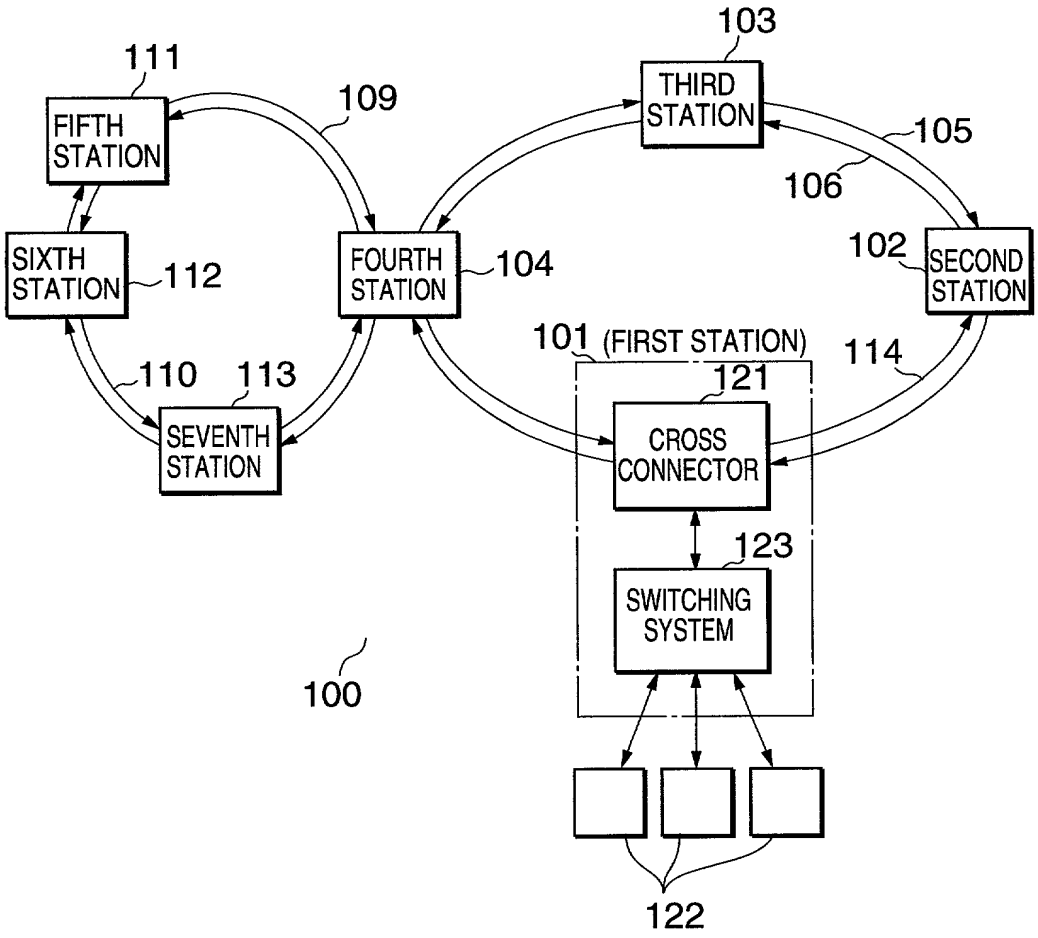

FIG. 1
PRIOR ART

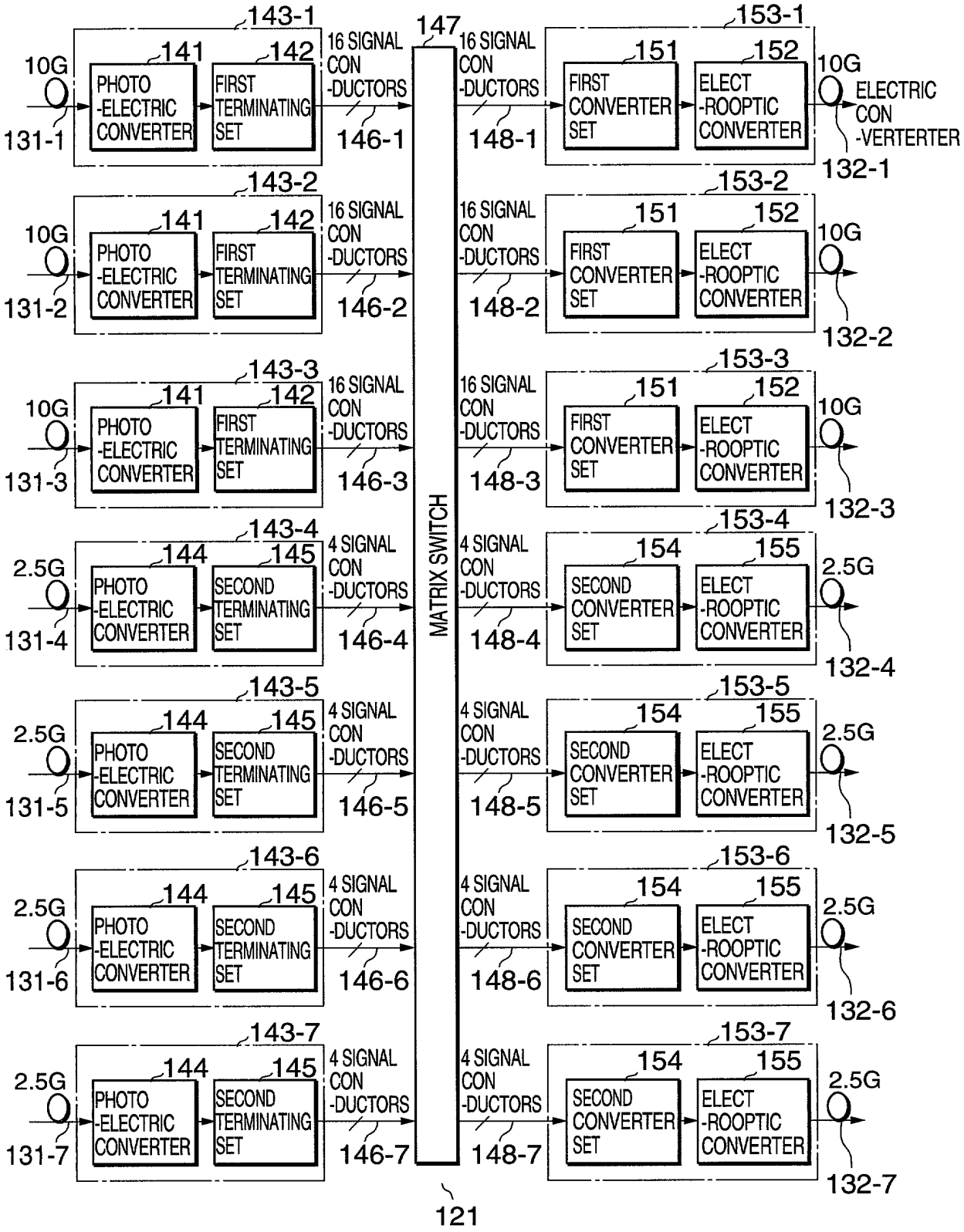

FIG. 2
PRIOR ART

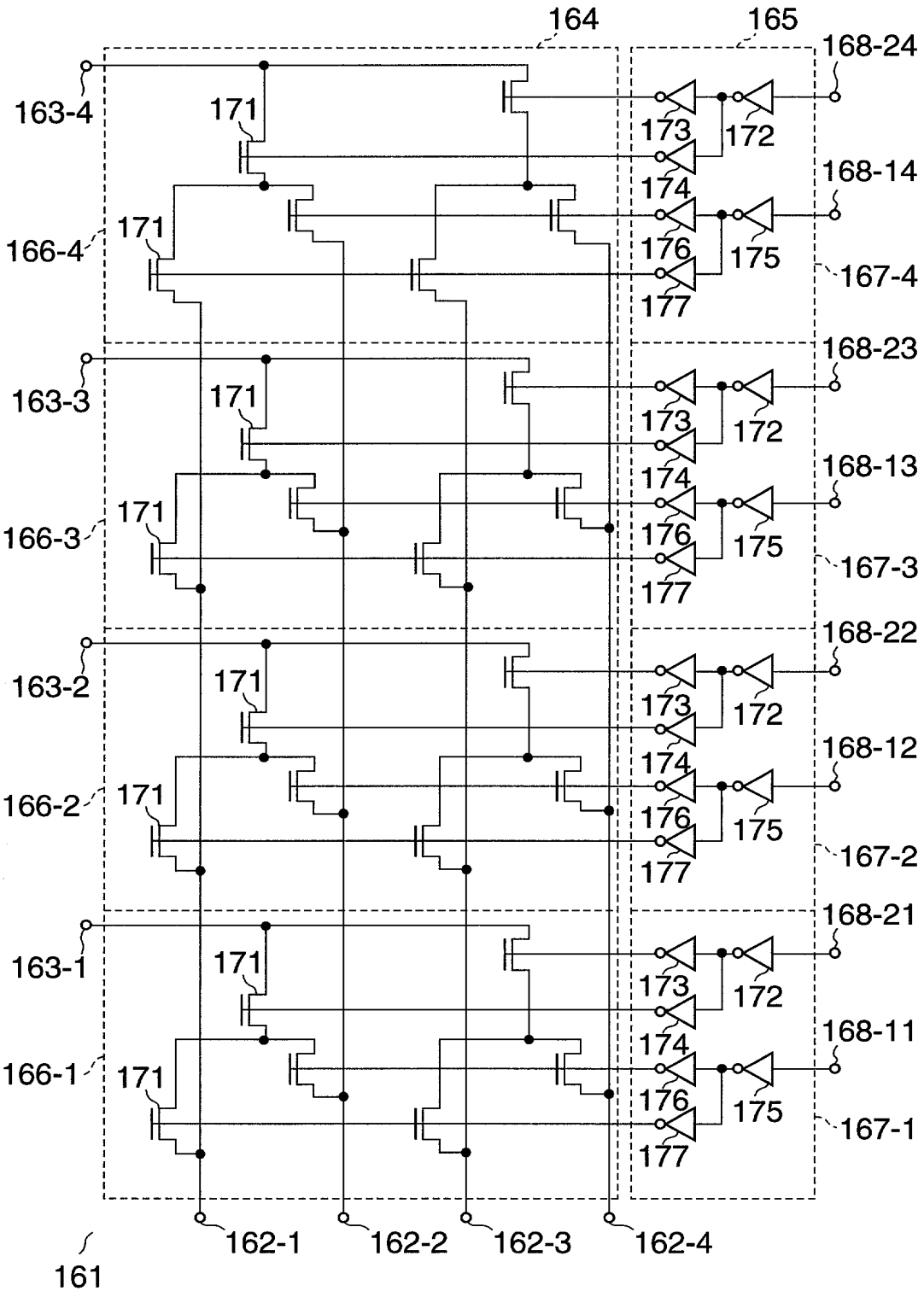

FIG. 3
PRIOR ART

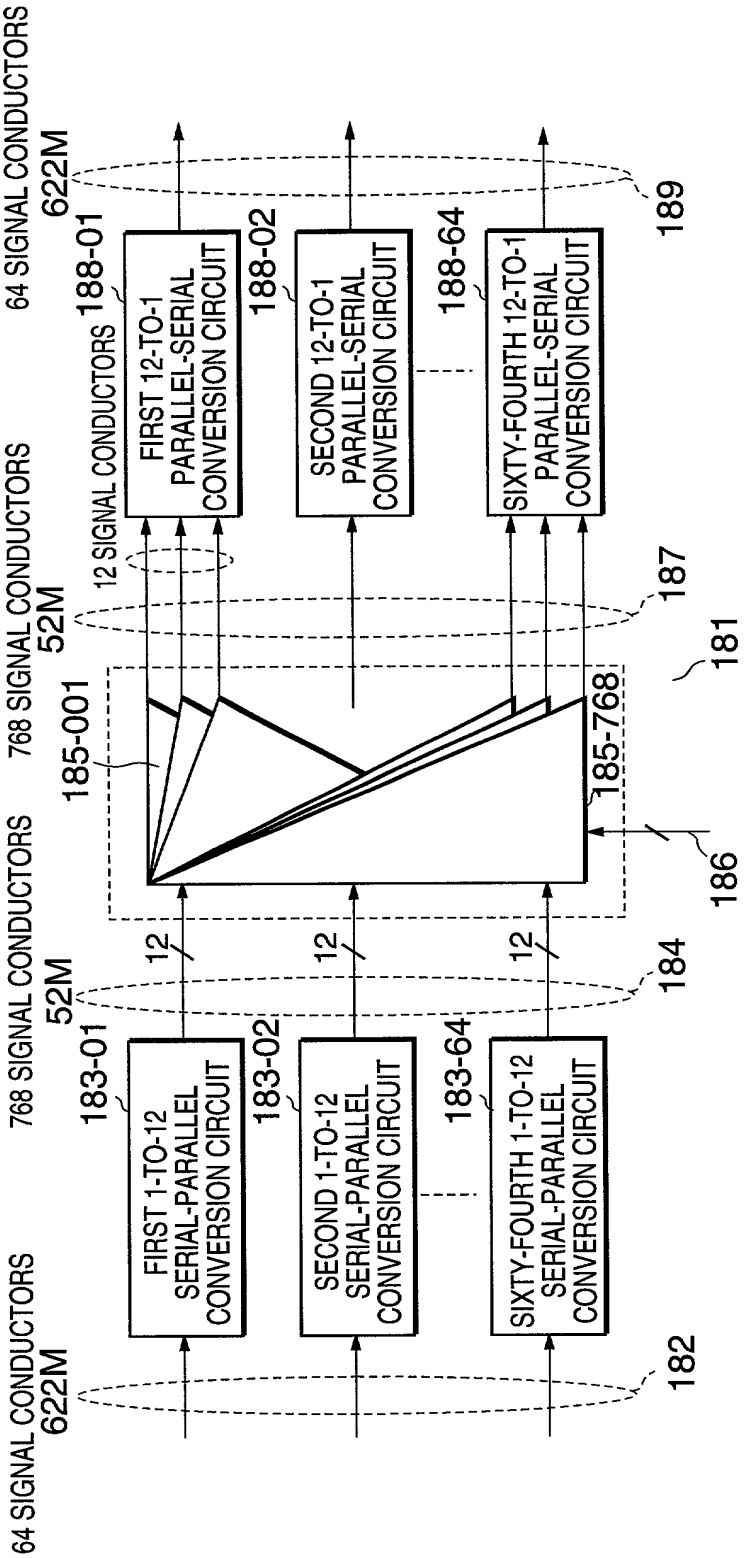

FIG. 4
PRIOR ART

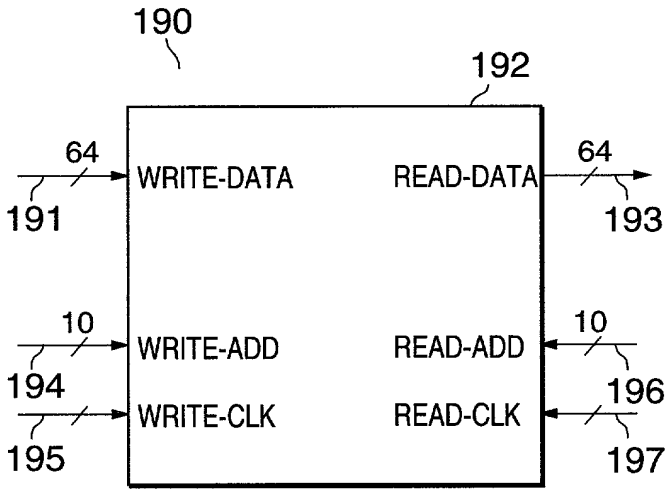

FIG. 5
PRIOR ART

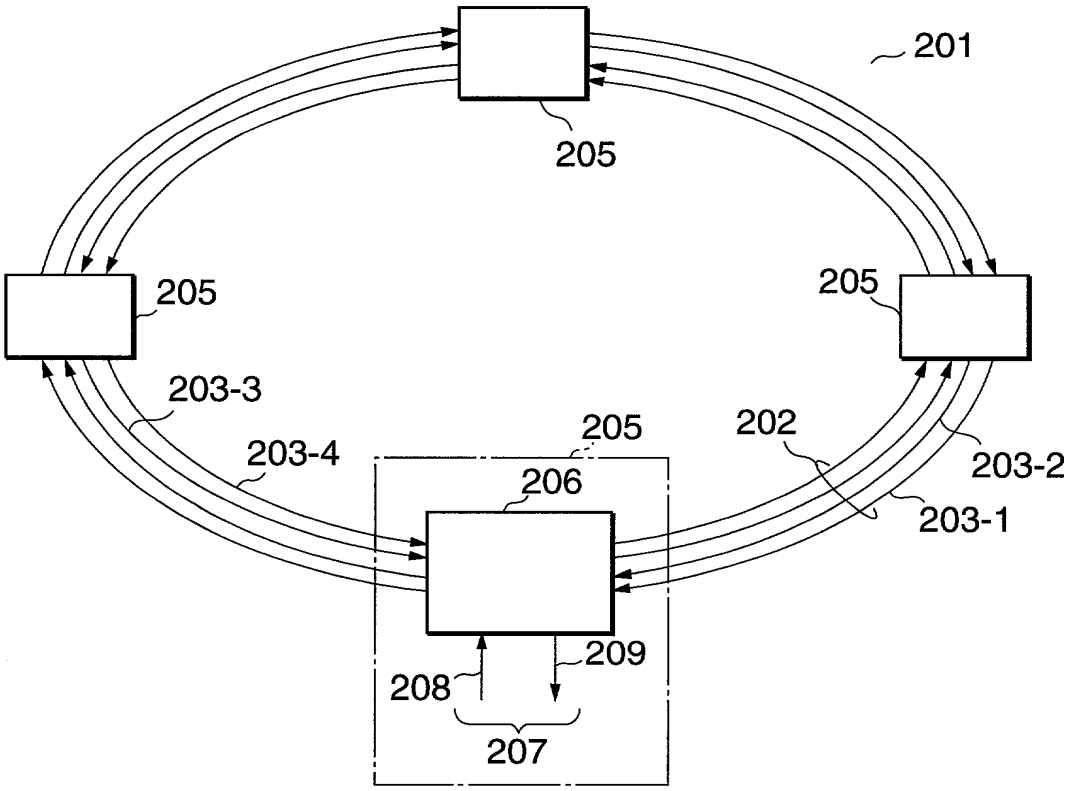

FIG. 6

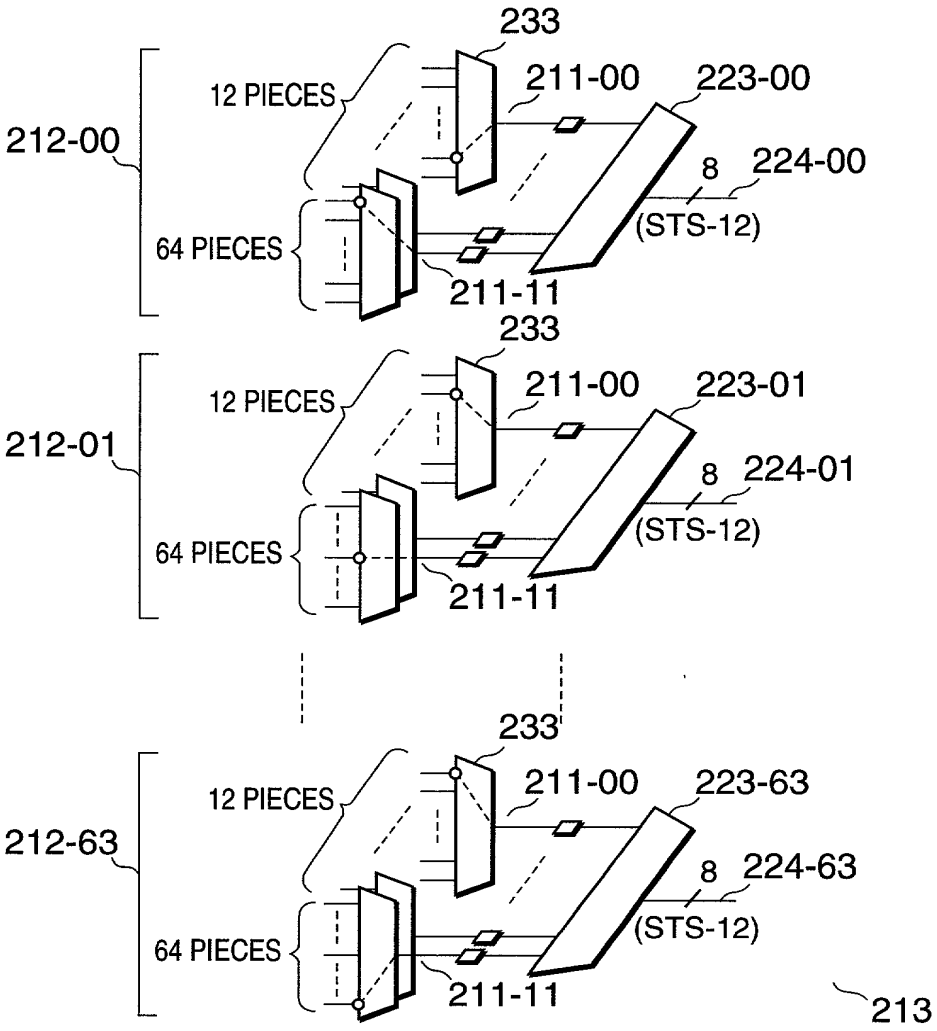
233
211-00
223-00
12 PIECES
212-00
8
224-00
(STS-12)
64 PIECES
211-11
233
211-00
223-01
12 PIECES
212-01
8
224-01
(STS-12)
64 PIECES
211-11
233
211-00
223-63
12 PIECES
212-63
8
224-63
(STS-12)
64 PIECES
211-11
213

FIG. 7

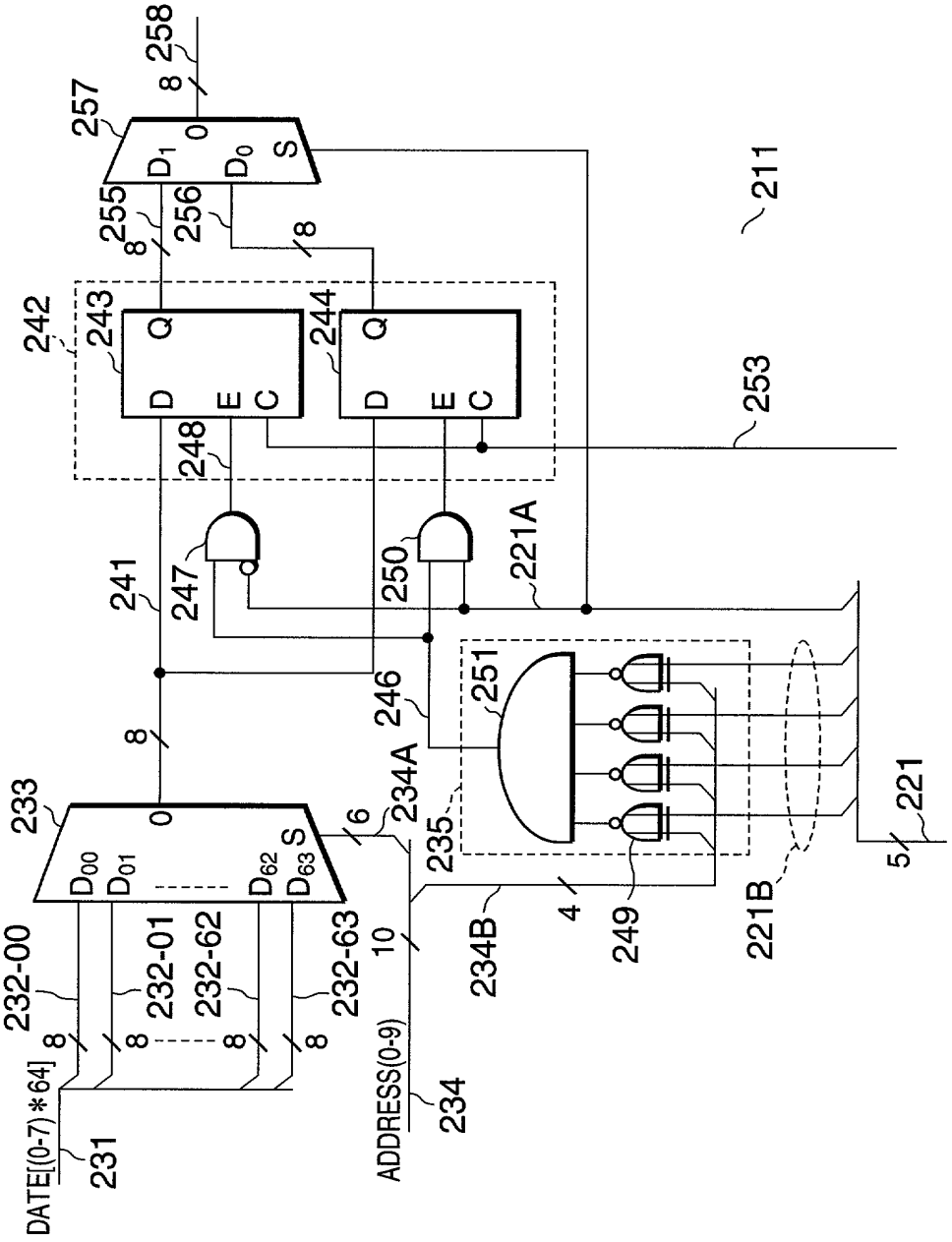
257
258
8
0
D1
D0
S
255
256
8
8
211
242
243
244
Q
D
E
C
253
248
241
247
250
221A
246
251
234A
235
233
0
6
D00
D01
D62
D63
S
232-00
232-01
232-62
232-63
8
10
4
5
234B
249
221B
221
DATE[(0-7)*64]
231
ADDRESS(0-9)
234

FIG. 8

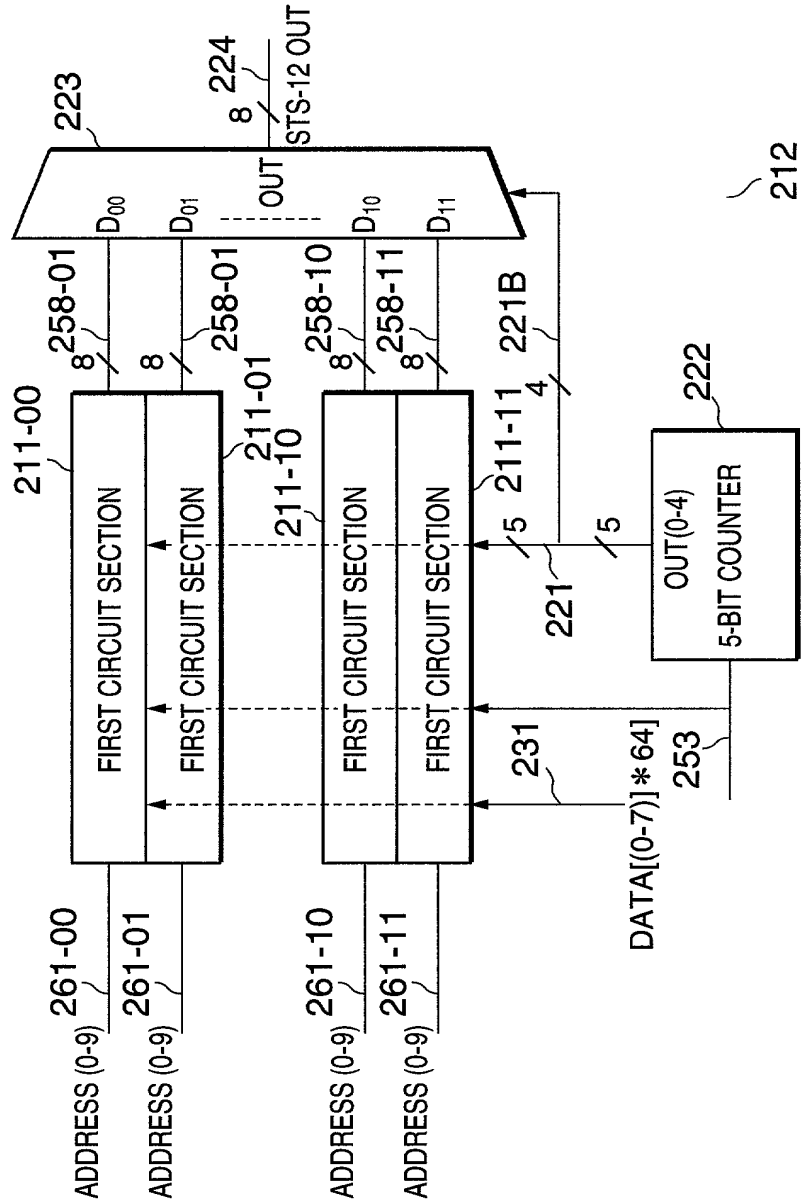
223
224
8
STS-12 OUT
OUT
D00
D01
D10
D11
212
258-01
258-01
258-10
258-11
221B
8
8
8
8
4
211-00
211-01
211-10
211-11
FIRST CIRCUIT SECTION
FIRST CIRCUIT SECTION
FIRST CIRCUIT SECTION
FIRST CIRCUIT SECTION
5
5
221
222
OUT(0-4)
5-BIT COUNTER
231
253
DATA[(0-7)] * 64]
261-00
261-01
261-10
261-11
ADDRESS (0-9)
ADDRESS (0-9)
ADDRESS (0-9)
ADDRESS (0-9)

FIG. 9

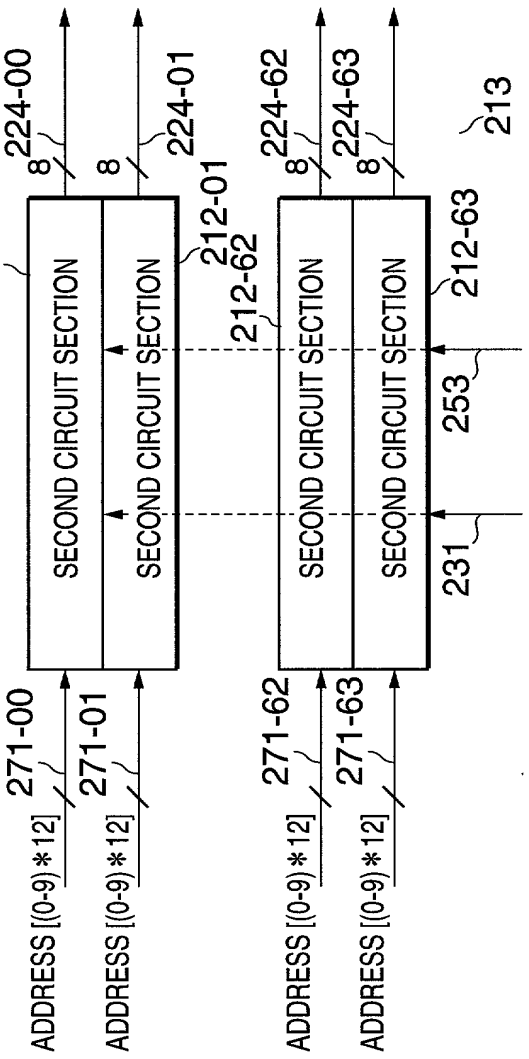
212-00
212-01
212-62
212-63
SECOND CIRCUIT SECTION
224-00
224-01
224-62
224-63
8
213
253
231
271-00
271-01
271-62
271-63
ADDRESS [(0-9)*12]

FIG. 10

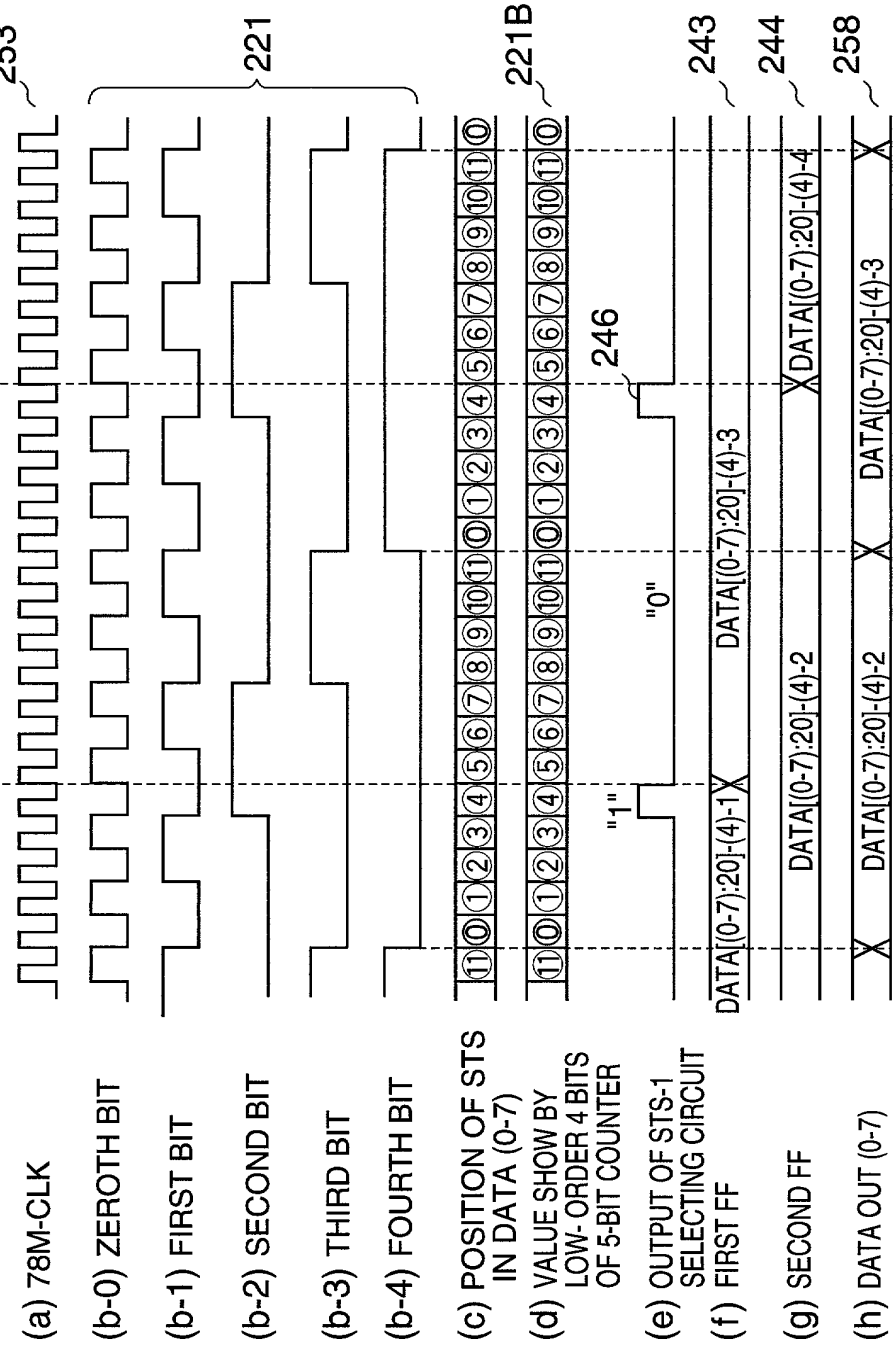
253
221
221B
243
244
258
246
t_1
(a) 78M-CLK
(b-0) ZEROTH BIT
(b-1) FIRST BIT
(b-2) SECOND BIT
(b-3) THIRD BIT
(b-4) FOURTH BIT
(c) POSITION OF STS IN DATA (0-7)
(d) VALUE SHOW BY LOW- ORDER 4 BITS OF 5-BIT COUNTER
(e) OUTPUT OF STS-1 SELECTING CIRCUIT
(f) FIRST FF
(g) SECOND FF
(h) DATA OUT (0-7)
"1"
"0"
DATA[(0-7):20]-(4)-1
DATA[(0-7):20]-(4)-3
DATA[(0-7):20]-(4)-2
DATA[(0-7):20]-(4)-4
DATA[(0-7):20]-(4)-2
DATA[(0-7):20]-(4)-3

FIG. 11

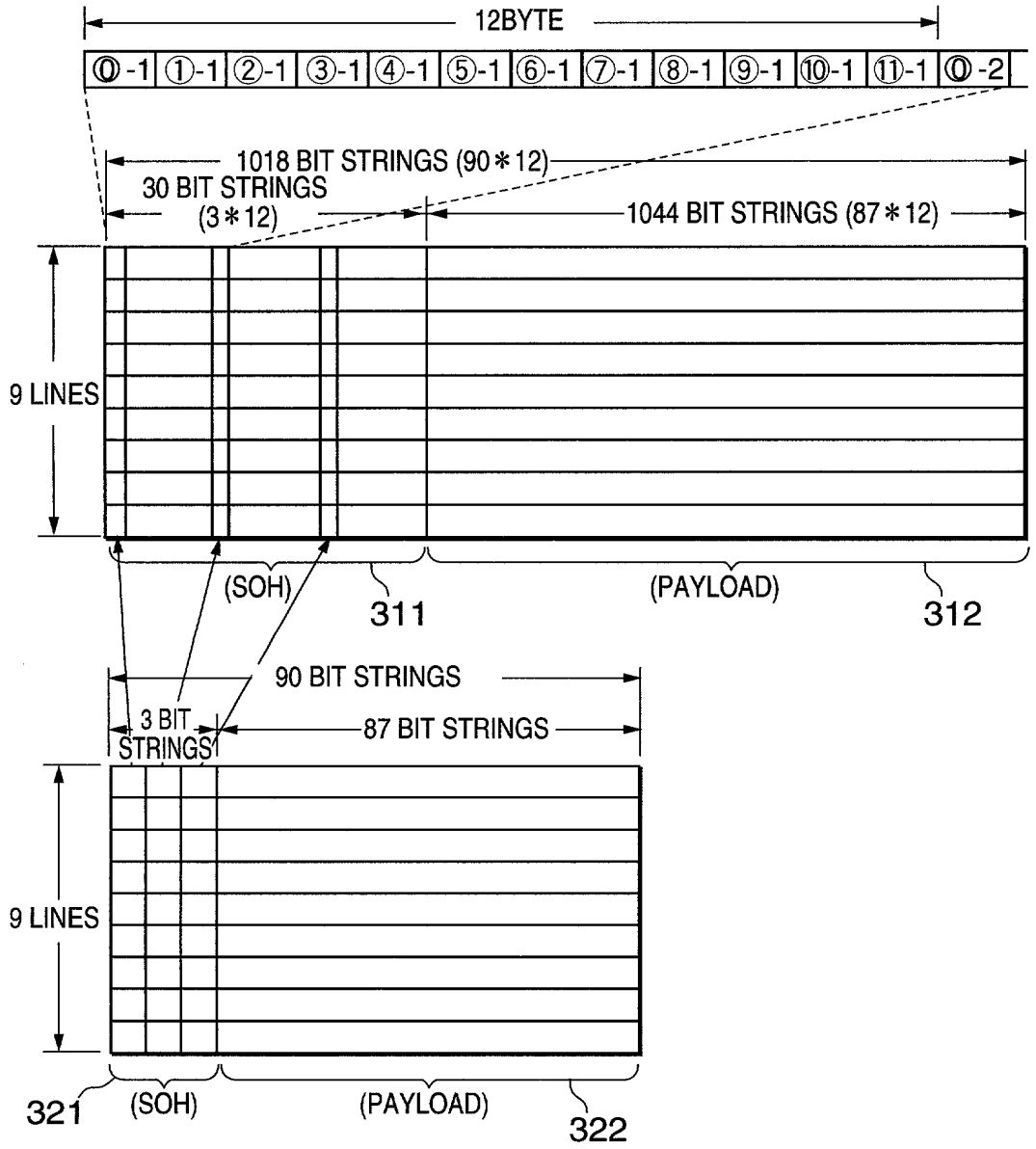
12BYTE
⓪-1
①-1
②-1
③-1
④-1
⑤-1
⑥-1
⑦-1
⑧-1
⑨-1
⑩-1
⑪-1
⓪-2
1018 BIT STRINGS (90*12)
30 BIT STRINGS (3*12)
1044 BIT STRINGS (87*12)
9 LINES
(SOH)
311
(PAYLOAD)
312
90 BIT STRINGS
3 BIT STRINGS
87 BIT STRINGS
9 LINES
321
(SOH)
(PAYLOAD)
322

FIG. 12

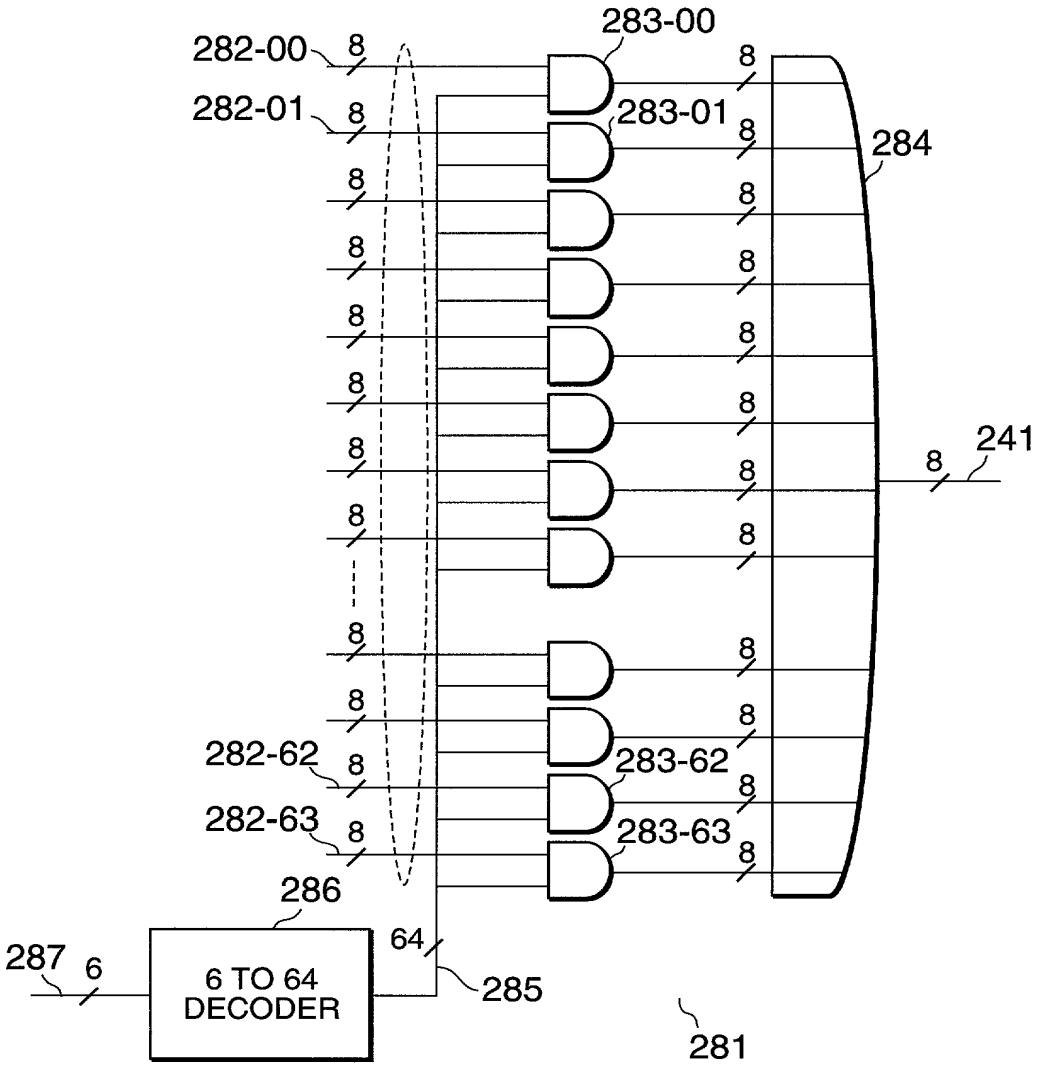
282-00
282-01
282-62
282-63
283-00
283-01
283-62
283-63
284
241
286
287
6
6 TO 64
DECODER
64
285
281
8

FIG. 13

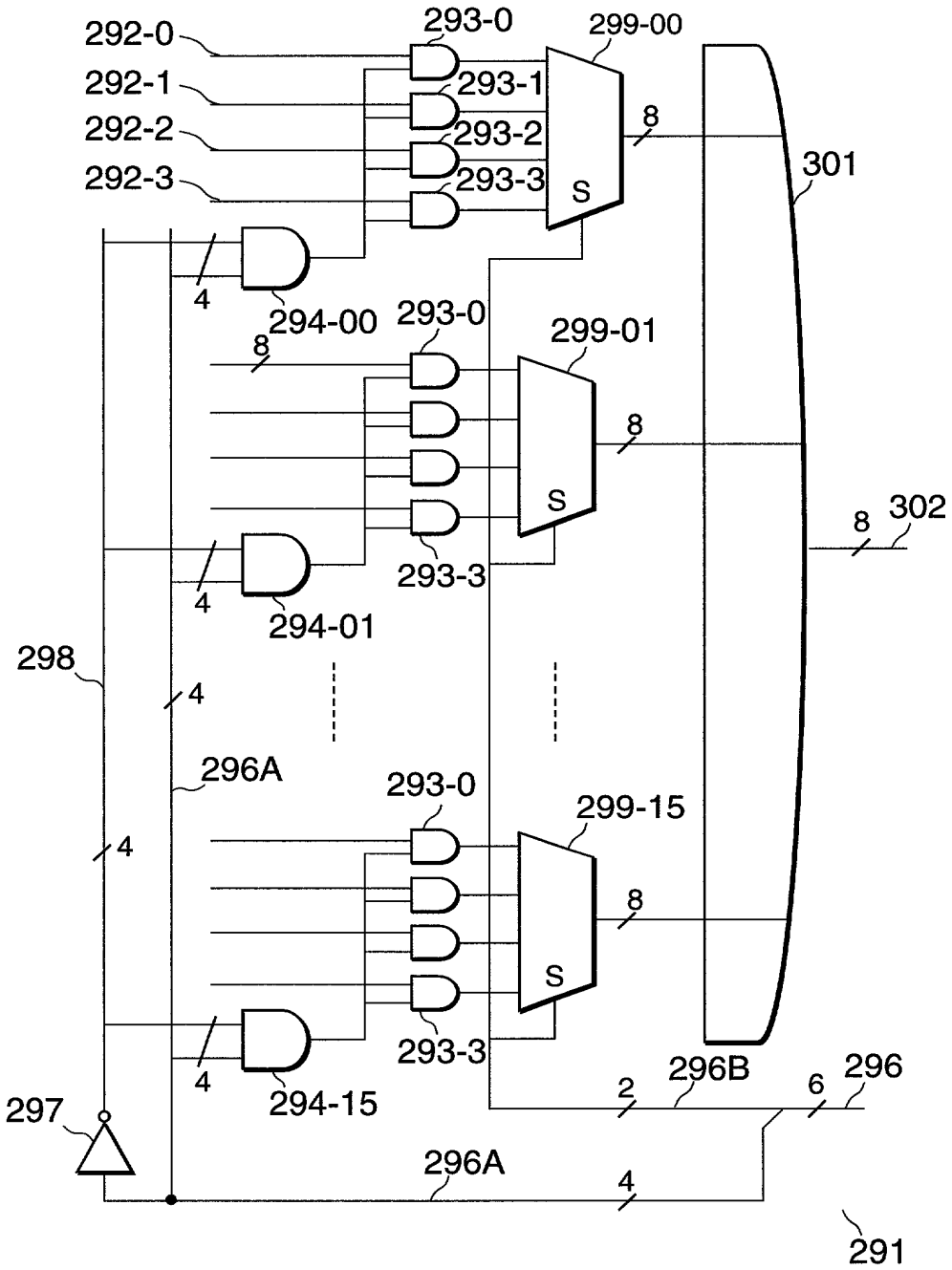
292-0
292-1
292-2
292-3
293-0
293-1
293-2
293-3
299-00
299-01
299-15
S
8
301
302
294-00
294-01
294-15
4
298
296A
296B
296
297
291

FIG. 14

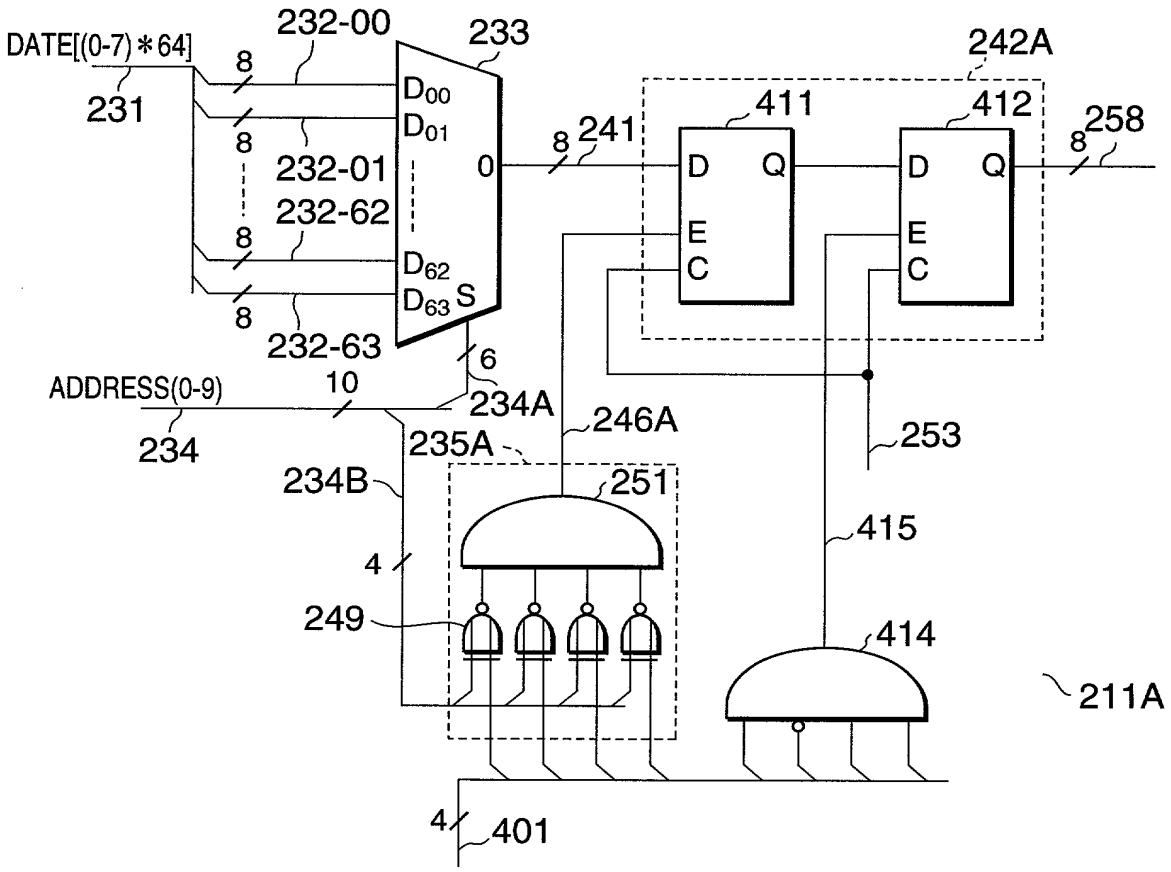
DATE[(0-7)*64]
231
8
232-00
232-01
232-62
232-63
233
D00
D01
D62
D63
S
0
6
ADDRESS(0-9)
10
234
234A
234B
235A
246A
241
242A
411
412
D
Q
E
C
258
253
415
414
211A
251
249
4
401

FIG. 15

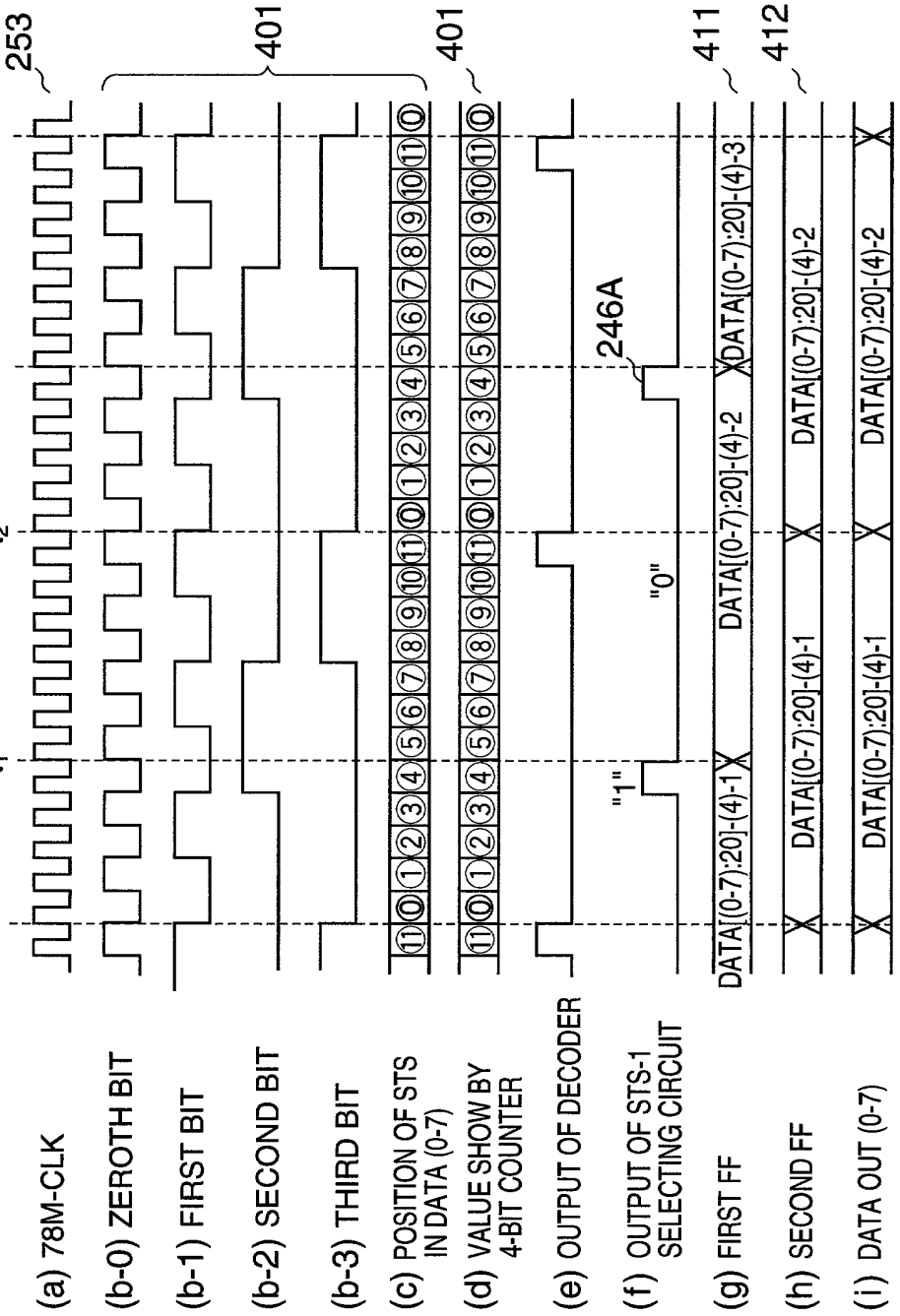
253
401
401
411
412
246A
t1
t2
(a) 78M-CLK
(b-0) ZEROTH BIT
(b-1) FIRST BIT
(b-2) SECOND BIT
(b-3) THIRD BIT
(c) POSITION OF STS IN DATA (0-7)
(d) VALUE SHOW BY 4-BIT COUNTER
(e) OUTPUT OF DECODER
(f) OUTPUT OF STS-1 SELECTING CIRCUIT
(g) FIRST FF
(h) SECOND FF
(i) DATA OUT (0-7)
"1"
"0"
DATA[(0-7):20]-(4)-1
DATA[(0-7):20]-(4)-2
DATA[(0-7):20]-(4)-3

FIG. 16

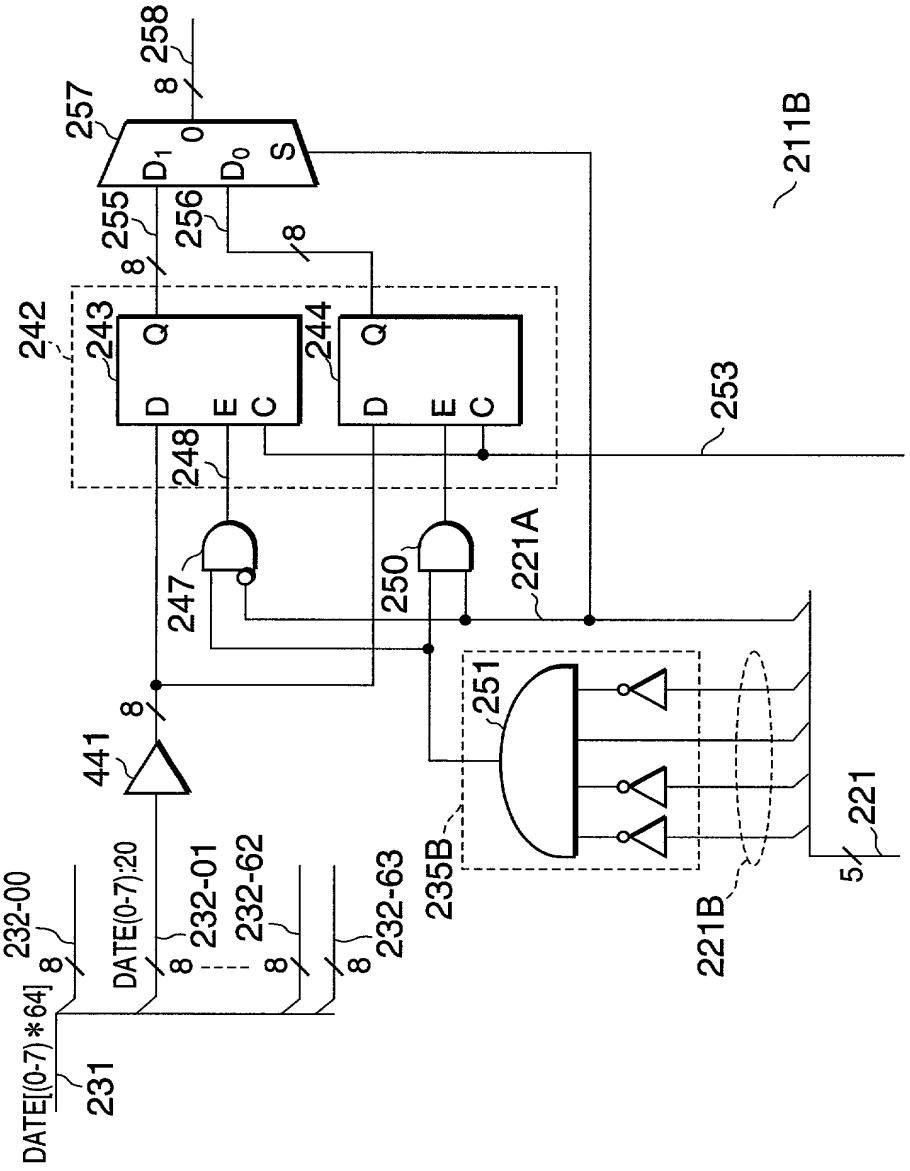
258
257
D1
0
D0
S
211B
255
256
8
242
243
244
Q
D
E
C
253
248
247
250
221A
441
251
235B
221
5
221B
232-00
DATE(0-7):20
232-01
232-62
232-63
DATE[(0-7)*64]
231

FIG. 17

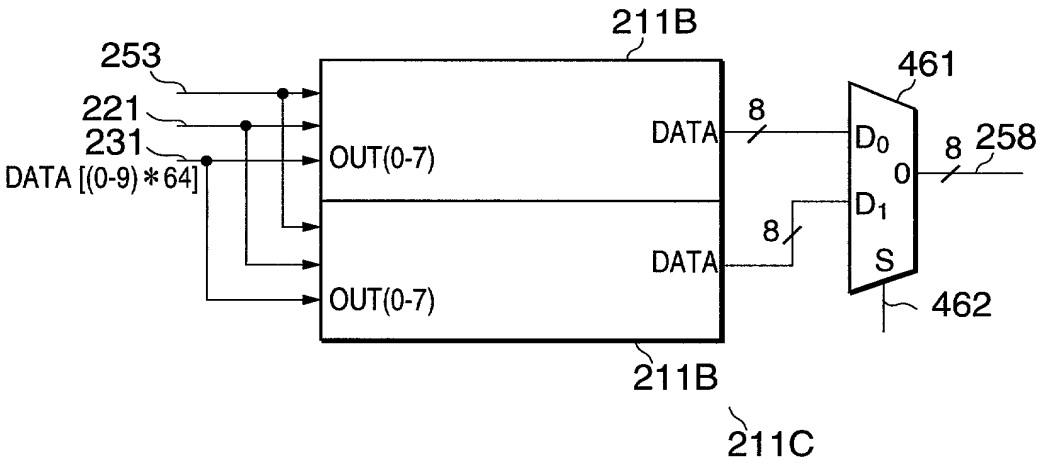
211B
253
221
231
DATA [(0-9)*64]
OUT(0-7)
OUT(0-7)
DATA
DATA
8
8
461
D0
D1
S
0
8
258
462
211B
211C

FIG. 18

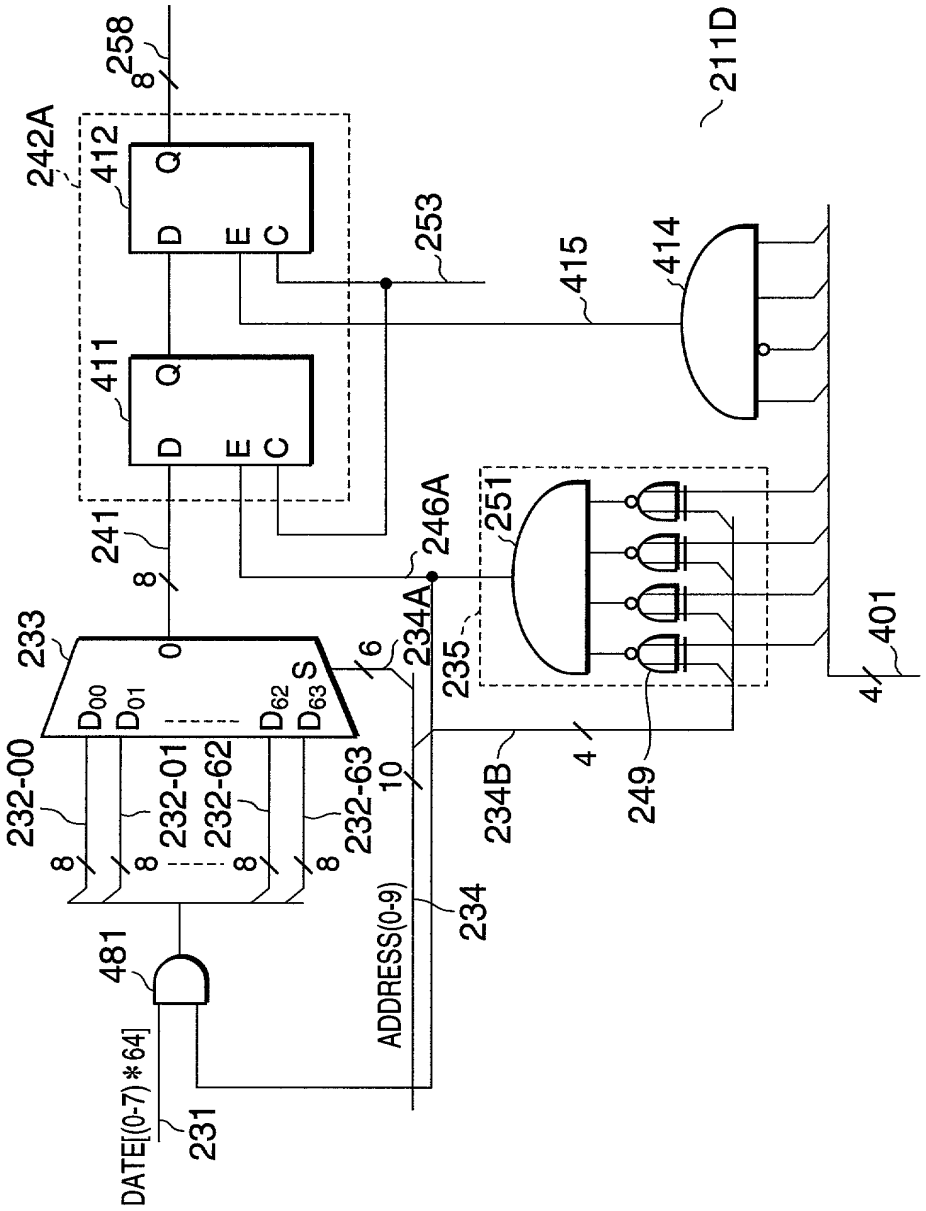
258
8
242A
412
Q
D
E
C
411
Q
D
E
C
253
415
414
211D
241
8
246A
251
233
0
6
234A
235
401
4
D00
D01
D62
D63
S
232-00
232-01
232-62
232-63
8
10
234B
4
249
481
234
ADDRESS(0-9)
DATE[(0-7)*64]
231

FIG. 19

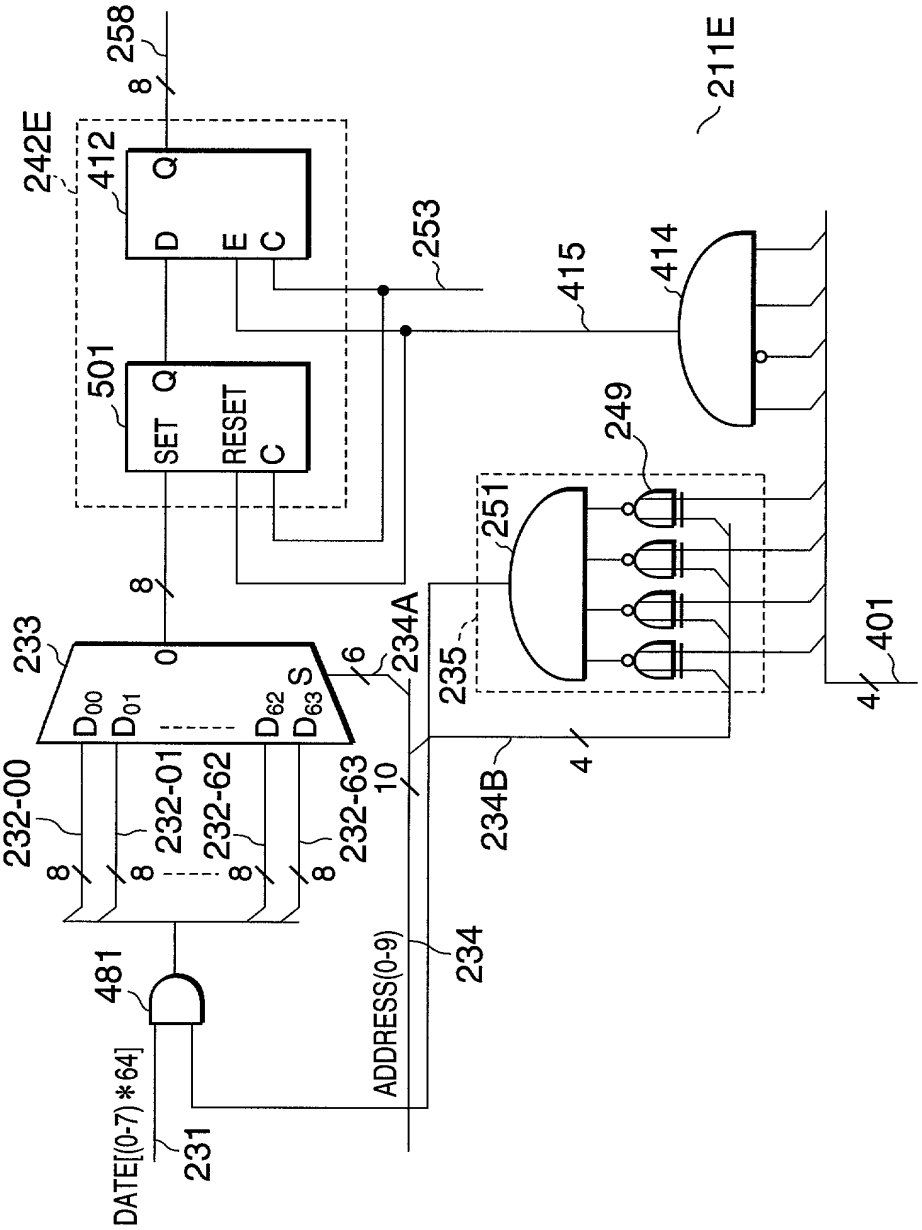
258
8
242E
412
Q
D
E
C
253
211E
501
SET
RESET
415
414
249
251
8
233
0
6
234A
235
401
4
D_{00}
D_{01}
D_{62}
D_{63}
S
232-00
232-01
232-62
232-63
10
234B
4
8
481
234
ADDRESS(0-9)
DATE[(0-7)*64]
231

FIG. 20

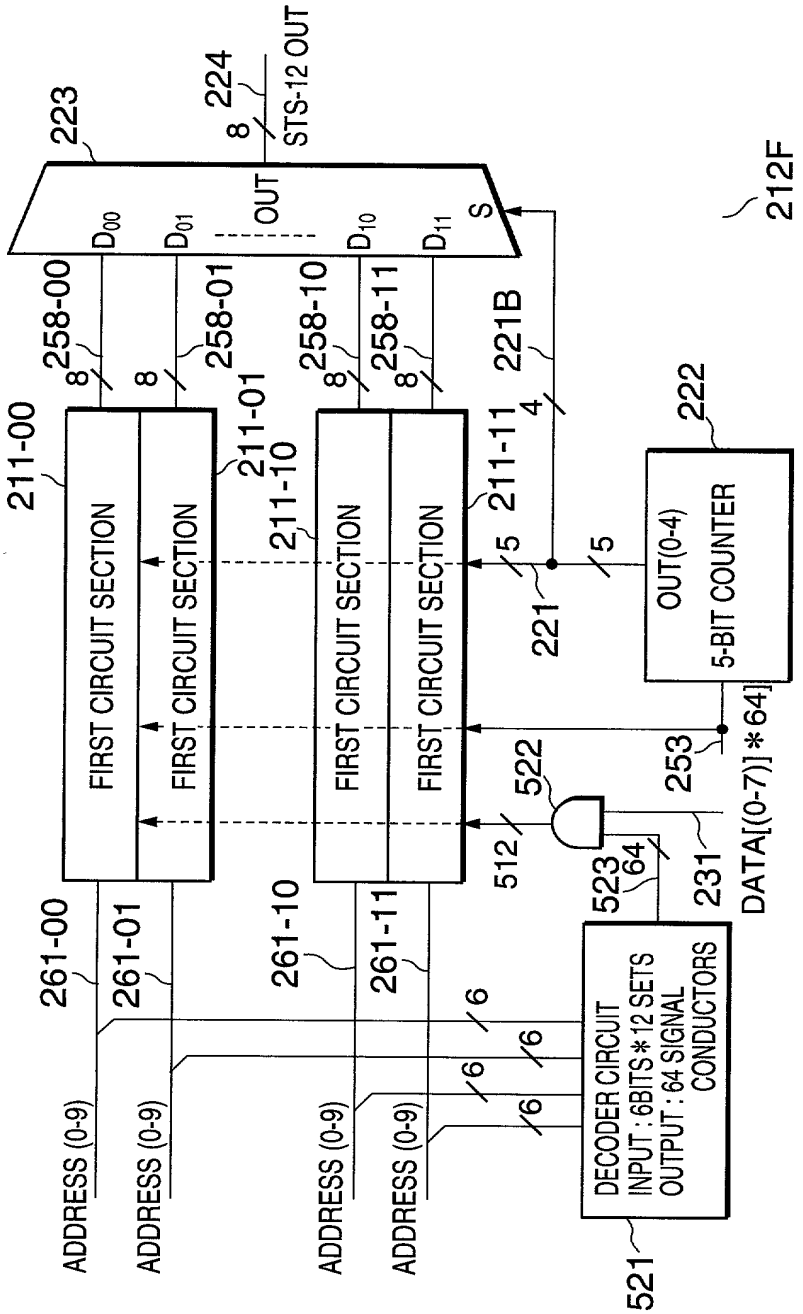
223
224
8
STS-12 OUT
OUT
D_{00}
D_{01}
D_{10}
D_{11}
S
212F
258-00
258-01
258-10
258-11
8
221B
4
211-00
211-01
211-10
211-11
FIRST CIRCUIT SECTION
5
221
222
OUT(0-4)
5-BIT COUNTER
253
DATA[(0-7)] * 64]
522
512
523
64
231
261-00
261-01
261-10
261-11
6
ADDRESS (0-9)
DECODER CIRCUIT
INPUT : 6BITS * 12 SETS
OUTPUT : 64 SIGNAL
CONDUCTORS
521

FIG. 21

	SYSTEM SHOWN IN FIG. 8	SYSTEM SHOWN IN FIG. 9	SYNTHESIS BY MINIMIZING SCALE BY LOGICAL SYNTHESIS
POWER CONSUMPTION (mW)	120	180	934
CIRCUIT SCALE (M GATE)	0.94	1.6	1.1

FIG. 22

	SYSTEM SHOWN IN FIG. 8	SYSTEM SHOWN IN FIG. 9	SYNTHESIS BY MINIMIZING SCALE BY LOGICAL SYNTHESIS
POWER CONSUMPTION (mW)	20	30	156
CIRCUIT SCALE (M GATE)	1.2	1.6	1.3

FIG. 23

	SYSTEM SHOWN IN FIG. 8	SYSTEM SHOWN IN FIG. 9	SYNTHESIS BY MINIMIZING SCALE BY LOGICAL SYNTHESIS
POWER CONSUMPTION (mW)	120	180	187
CIRCUIT SCALE (M GATE)	1.0	1.4	1.2

FIG. 24